IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

application of:

GELINAS et al.

Appl. No.: 09/637,500

Filed: August 11, 2000

For: High Performance RISC Instruction Set Digital Signal Processor Having Circular Buffer and Looping Controls

(as amended)

Confirmation No.: 7608

Art Unit: 2181

Examiner: Tsai, Henry

Atty. Docket: 1778.2090001

Information Disclosure Statement

Mail Stop RCE

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

Sir:

Listed on accompanying IDS Forms are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Applicants have listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

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This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on

Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

Copies of documents NPL1-NPL4 are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application publications cited on the attached IDS Forms are submitted.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Virgil L. Beaston

Attorney for Applicants Registration No. 47,415

Date: September 27, 2006

the material submitted herewith.

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Application Number	09/637,500			
Filing Date	August 11, 2000			
First Named Inventor	Robert GELINAS			
Art Unit	2181			
Examiner Name	Tsai, Henry			
Attorney Docket Number	1778.2090001			

-			U.S. PATENT DO	CUMENTS		
Examiner		Document Number	Publication Date	Name of Patentee or	Pages, Columns, Lines,	
Initials* No.1	Number-Kind Code ^{2 (If Known)}	MM-DD-YYYY	Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear		
	US1	5,864,703	01-26-1999	van Hook et al.		
	US2	5,933,650	08-03-1999	van Hook et al.		
	US3	6,266,758 B1	07-24-2001	van Hook et al.		
	US4	2002/0062436 A1	05-23-2002	van Hook et al.		
	US5	2006/0129787 A1	06-15-2006	van Hook <i>et al</i> .		
	US6					
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English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Filing Date	August 11, 2000			
		First Named Inventor	Robert GELINAS			
		Art Unit	2181			
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		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL1	Gwennap, L., "Digital, MIPS Add Multimedia Extensions: Digital Focuses on Video, MIPS on 3D Graphics; Vendors Debate Differences," <i>Microprocessor Report</i> , Vol. 10, No. 15, pp. 1-5 (November 18, 1996).	
	NPL2	Gwennap, L., "New Multimedia Chips to Enter the Fray: Media Processors, Multimedia-Enhanced CPUs Debut at Microprocessor Forum," <i>Microprocessor Report</i> , Vol. 10, No. 13, 1 page (October 7, 1996).	
	NPL3	Killian, E., "MIPS Extensions for Digital Media," <i>Microprocessor Forum</i> , pp. 1-5 (October 22-23, 1996).	
	NPL4	van Hook, T.J. et al., U.S. Patent Appl. No. 09/662,832, entitled "Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing," 60 pages, as filed September 15, 2000.	
	NPL5		
	NPL6		
	NPL7		
	NPL8		
	NPL9		
	NPL10		

Examiner	Date
Signature	Considered

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